REMARKS

Claims 1, 4-10, 13-17, 20, 21. and 22 are presently pending. Claims 1, 4-10, 13-17, 20, and 21 are rejected. Claim 22 is added.

Claim 1, 9, and 17 were rejected under 35 U.S.C. 103(a) as being obvious from the combination of Jones in view of Gelsomini. Claim 20 was rejected as being obvious from the combination of Jones, Gelsomini, and Khoury. Claim 21 was rejected under 35 U.S.C. § 103(a) as being obvious from the combination of Jones in view of Gelsomini, and further in view of Giolma.

Claim 1 recites, among other limitations, "wherein the element comprises a thin oxide gated fuse having an oxide that is less than 2.5nm thick". The Office Action has indicated that "JONES does not disclose that the element comprises a thin gated fuse having a oxide that is less than 2.5 nm thick and the state of the element is a state of the electrical resistance of the element. GELSOMINI discloses a thin oxide gate fuse (as described in paragraph 50 of the instant application) having an oxide that is less than 2.5nm thick (see for example column 4, lines 2-6 and claim 5)...". Office Action at 4.

Gelsomini teaches "Gate oxide anti-fuses have gate insulators made of silicon dioxide in a thickness range from about 2 to 10nm." Col. 4, Lines 3-4. The Office Action also cites MPEP 2144.05.I. Although the claimed range < 2.5nm and the range disclosed in Gelsomini, 2-10nm overlap, "Applicants can rebut a *prima facie* case of obviousness based on overlapping ranges by showing the criticality of the claimed range. 'The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.' *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990)." MPEP 2144.05.III.

Assignee respectfully submits that the claimed range, < 2.5nm achieves unexpected results relative to the prior art range. Paragraph 0011 of 09/739,752, which is incorporated by reference in the present application, 0009, "The oxide is about 20 Angstroms thick, which allows direct tunneling current and yields an after-programmed resistance on the order of a few hundred ohms or less, *which is an order of magnitude lower then conventional one-time programmable anti-fuses*. Voltage to rupture gate

oxide can be adjusted depending on the programming time pulse and final resistance spread requirement." Additionally, paragraph 0029 of 09/739,752 states that the claimed range has properties not possessed by the prior art, "The gate oxide layer is approximately 20 Angstroms thick, which can be achieved with 0.13 um or less process technology. This thickness is chosen so that the gate can be ruptured by direct tunneling gate current, rather than Fowler-Nordheim tunneling." "Presence of a property not possessed by the prior art is evidence of nonobviousness. *In re Papesch*, 315 F.2d 381, 137 USPQ 43 (CCPA 1963). MPEP 716.02(a).

Accordingly, Assignee respectfully traverses the rejection to claims 1, 9, 17, and 20 as obvious from the combination of Jones in view of Gelsomini.

Additionally, claim 1 recites, among other limitations, "determining if the state of the element is equal to an expected state using a verify circuit, wherein the state of the element is a state of the electrical resistance of the element". The Office Action indicates that Jones discloses "determining if the state of the element is equal to an expected state (VERIFY DATA 0 in Fig. 3b) using a verify circuit (308 in Fig. 3a); and outputting a valid signal (FAST VERIFY OUTPUT of 390 in Fig. 3b) if the state of the element is equal to said expected state (if DR0 is equal to VERIFY DATA 0 in Fig. 3b;". Examiner has also indicated that Gelsomini teaches "a thin oxide gated fuse … wherein a state of the fuse is a state of the electrical resistance of the fuse (inherent as a fuse)." Examiner also indicated that "It would be obvious at the time the invention was made … to substitute a thin oxide gated fuse … as an equivalent memory element … such that the state of the element is a state of the electrical resistance of the element".

Assignee respectfully traverses the rejection because Jones and Gelsomini do not teach "determining if the state of the element is equal to an expected state using a verify circuit, wherein the state of the element is a state of the electrical resistance of the element". Structure 308, which Examiner has indicated that the "verify circuit" which is used for "determining if the state of the element (DR0 in Fig. 3b) is equal to an expected state (VERIFY DATA 0 in Fig. 3b) are (further illustrated in Figure 3b) XOR gates. While XOR gates measure signals – the XOR gates do not measure electrical resistance.

Examiner has responded that "when Gelsomini's fuse/antifuse is substituted for the memory element in the Jones/Gelsomini combination, in obtaining the VERIFY

DATA 0 signal in Fig. 3b of Jones, although it may be a logic signal, it is inherently determined by, or based on a state of the electrical resistance/conductivity of the fuse/antifuse.

Assignee respectfully traverses. As an initial matter, Examiner provides no reasoning as to why VERIFY DATA 0 signal is inherently based on a state of the electrical resistance/conductivity of the fuse/antifuse. Secondly, it is not inherent. VERIFY DATA 0 is the output of an XOR gate. The output of an XOR gate is entirely determined by the signal levels of the inputs. Moreover, the output of the XOR gate would reveal the state of the electrical resistance of the fuse/antifuse. For example, if the fuse/antifuse is in a state of zero electrical resistance, the output of the XOR gate can still be either 0 or 1. Accordingly, the an XOR gate, element 308 is inoperable to determine "if the state of the element is equal to an expected state using a verify circuit, wherein the state of the element is a state of the electrical resistance of the element".

For the reasons above, Assignee respectfully submit that the combination of Jones, and Gelsomini do not teach or fairly suggest "wherein the state is a state of electrical resistance". Accordingly, Examiner is requested to withdraw the rejection to claims 1, 9, 17, and 20 as well as to dependent claims 4-8, 10, 13-16, 21 and 22.

Additionally, newly added claim 22 recites, among other limitations, "wherein the thin oxide gated fuse having an oxide that is less than 2 nm thick." Assignee respectfully submits that the combination of Jones and Gelsomini does not teach the foregoing limitation.

Conclusion

For at least the foregoing reasons, each of the pending claims are in a condition for allowance.

The Office Action makes various statements regarding the claims and the cited references that are now moot in view of the above amendments and/or arguments. Thus, the Applicant will not address all of such statements at the present time. However, the Applicant expressly reserves the right to challenge such statements in the future should the need arise (e.g., if such statements should become relevant by appearing in a rejection of any current or future claim).

Please charge any required fees not paid herewith or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.In view of the foregoing, it is respectfully submitted that the pending claims define allowable subject matter. Should anything remain in order to place the present application in condition for allowance, the Examiner is kindly invited to contact the undersigned at the telephone number listed below.

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Respectfully submitted,

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